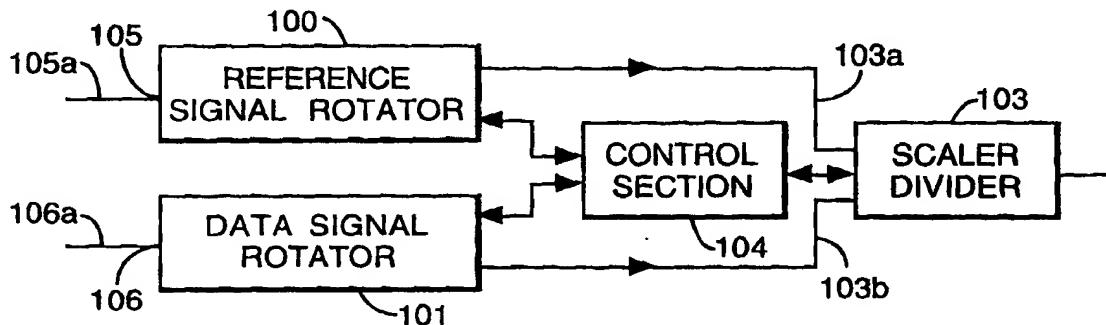




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(71) Applicant (for all designated States except US): NDS LIMITED [GB/GB]; 1 Heathrow Boulevard, 286 Bath Road, West Drayton, Middlesex UB7 0DQ (GB).			
(72) Inventor; and			
(75) Inventor/Applicant (for US only): TURNER, Adrian, Charles [GB/GB]; 17 Northdene Road, Chandlers Ford, Eastleigh, Hampshire SO53 3DW (GB).			
(74) Agent: ANDERSON, Angela, NDS Limited, Stoneham Rectory, Stoneham Lane, Eastleigh SO50 9NW (GB).			

(54) Title: CORRECTION OF PHASE AND AMPLITUDE DISTORTION, PARTICULARLY FOR MULTICARRIER SIGNALS



(57) Abstract

This invention relates generally to receiving frequency division multiplex signals, and, more precisely, to a method and apparatus of receiving orthogonal frequency division multiplex signals. OFDM signals may comprise both data and reference carriers (also known as pilots). The pilot signals are transmitted with a known phase and amplitude, however when they are received at a receiver the phase and amplitude is seldom as it was at the transmitter. This is due to problems of channel distortion which cause the phase and amplitude of the signals to be distorted. The same distortion also affects the data carriers, which can result in erroneous data being received. However, since the pilot signals are transmitted with a known phase and amplitude the distortion suffered by the pilot can be calculated, and the pilot can be rotated and re-scaled to recover its original phase and amplitude. Applying the same transformation to the data signals corrects them for any channel distortion. The present invention provides an effective method and apparatus for quickly and accurately recovering the amplitude and phase of an input signal.

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CORRECTION OF PHASE AND AMPLITUDE DISTORTION, PARTICULARLY FOR MULTICARRIER SIGNALS

5 The present invention relates to a method and apparatus for recovering the amplitude and phase of an input data signal. The invention is of particular application to recovering input data signals that are Orthogonal Frequency Division Multiplex (OFDM) signals.

10 In an OFDM receiver, the amplitude and phase of the received data signal must be recovered before de-mapping can take place. The channel amplitude and phase are recovered for each carrier position and the data is then corrected by this amount. This correction process requires a complex or vector division, sometimes known as 'projection'.

15 Complex division in its most straightforward form requires six full multiplications, three additions and two divisions. The process described here involves a modified CORDIC (CO-ordinate Rotation Digital Computer) process and two scalar dividers. Both are simple iterative processes that can

20 easily be pipelined and involve only adder/subtractors and multiplexers.

The CORDIC process is a well-established method of performing vector rotations. The accuracy of the result is dependent upon the number of iterations of the process: for n bits of accuracy, $n+1$ iterations are required.

25 Unfortunately the process does not converge very quickly and there may still be some residual error in the result.

30 The present invention now provides a method of recovering the amplitude and phase of an input data signal including at least one data vector and a reference vector, the method comprising the steps of rotating the reference vector, rotating the data vector by reference to the rotation of the reference vector and dividing the resultant data vector by the resultant reference vector.

The present invention also provides apparatus for recovering the amplitude and phase of an input data signal including at least one data vector and a reference vector comprising a means of rotating a reference vector, a means of rotating a data vector with reference to a reference vector and a means of scalar dividing two vectors.

In an OFDM receiver a pilot, or reference, signal is received which was transmitted with a known phase and a known amplitude. One or more data signals will also be received. Due to distortion caused by the transmission channel the received signals do not necessarily have the same phase or amplitude as when transmitted. To recover the phase and amplitude of the data signal, the reference signal is first rotated to its original transmitted position. The data signal is also rotated by the same amount, thus correcting it for phase distortion. A scalar division of the rotated data signal by the rotated reference signal then corrects the data signal for any distortion in amplitude.

The invention will now be described, by way of example, with reference to the accompanying drawings in which:

- 20 Figure 1 is a diagram showing an overview of the amplitude and phase recovery system according to the present invention;
- Figure 2 is a diagram showing a detailed view of the reference vector rotator according to the present invention;
- Figure 3 is a diagram showing a detailed view of the data vector rotator according to the present invention;
- 25 Figure 4 is a diagram showing a detailed view of the scalar divider according to the present invention;
- Figure 5 is a diagram showing a detailed view of the control section according to the present invention;
- 30 Figure 6a is a flow diagram showing the procedure performed by the first cycle of the control section according to the present invention;

Figure 6b is a flow diagram showing the procedure performed by the second and subsequent cycles of the control section according to the present invention;

Figure 7 is a diagram showing the rotation of a reference vector according to

5 the present invention.

In an OFDM receiver the amplitude and phase of the reference signal and the input data signal are converted into rectangular co-ordinates describing their respective vectors. The reference vector is known as the denominator (as it will ultimately be used to divide the data vector) and the data vector is known 10 as the numerator (as it will ultimately be divided by the reference vector).

Figure 1 shows an overview of the amplitude and phase recovery system according to the present invention. The co-ordinates of a received reference signal 105a are applied at an input 105 to a reference rotator 100. Similarly,

15 the co-ordinates of a received data signal 106a are applied at an input 106 to a data rotator 101. The received reference signal 105a undergoes distortions during transmission due to various channel distortions, but the parameters of this signal are known at transmission. The same distortions will also affect the data vector. To recover the phase of the data signal the reference rotator 100,

20 under control of control section 104, rotates the received reference signal 105a to the original known phase, thereby correcting any phase distortion.

The data rotator 101, under control of control section 104, rotates the received data signal 106a by the same amount as the received reference signal. This causes the received data signal 106a to be corrected for any 25 phase distortion due to the transmission channel. The phase corrected reference signal 103a and the phase corrected data signal 103b are subsequently input to a scalar divider 103.

The rotation stage can cause, however, an increase in amplitude of the 30 received signals. To correct for any increase in amplitude, the phase corrected data signal 103b is scalar divided by the phase corrected reference signal 103a. This is possible as, after correction, the phase corrected

reference signal 103a has a phase of 0 degrees. This means that dividing the phase corrected data signal 103b by the phase corrected reference signal 103a only affects the amplitude and results in correction of the amplitude of the phase corrected data signal.

5

The scalar divider 103 takes as inputs the phase corrected reference signal 103a and the phase corrected data signal 103b. The scalar divider 103, under the control of the control section 104, divides the phase corrected data signal 103b by the phase corrected reference signal 103a. The resultant signal, the 10 received data signal corrected for both phase and amplitude, is then output at 107 where it can be used by further stages of a receiver.

15 Figure 2 is a diagram showing a detailed view of the reference vector rotator according to the present invention. The received reference signal is input in its rectangular co-ordinate form with the X co-ordinate, X_d , being input at 2a and the Y co-ordinate, Y_d , being input at 2b.

20 The reference rotator comprises two adders, 8 and 9, which are controlled by way of an adder control signal 13, two shifters, 16 and 17, which are controlled by way of a shift control signal 30, two multiplexers, 20 and 21, which are controlled by way of a multiplex control signal 29, and another two multiplexers, 24 and 25, which are controlled by way of a load control signal 28. The control signals 13, 28, 29, 30 and 31 are supplied by control section 12 as shown in Figure 5. Additionally there are two registers, 4 and 5, which 25 are used to store the current X_d and Y_d values. The adder control signal, 13, is fed via an inverter, 14, before being input to adder 8. This has the effect that the adder 8 and the adder 9 are generally performing the opposite function - i.e. if the adder 8 is adding, the adder 9 is subtracting, and vice versa.

30

Depending on the value of the load control signal 28, the multiplexer 24 is used to either load in a new X co-ordinate into the register 4, or to load the

output of the adder 8 into the register 4. The multiplexer 25 performs the same operation for the Y co-ordinate and causes either a new Y co-ordinate or the output of the adder 9 to be loaded into the register 5, depending on the value of the load control signal 28.

5

Similarly, the multiplexer 20, under control of the multiplexer control signal 29, allows either a zero or the contents of the register 4 to be fed into the adder 8. The multiplexer 21, under control of the multiplexer control signal 29, allows either a zero or the contents of the register 5 to be fed into the adder 9.

10

The shift registers 16 and 17 shift their respective data to perform a division by 1, 2, 4, 8 etc. according to the value of the shift control signal 30.

15

The operation of the reference vector rotator is controlled by the control section 104, which is described in more detail below.

20

At the end of the rotation operation the X co-ordinate is output to the scalar divider section 103. The Y co-ordinate is not available as an output as it will always be zero at the end of the rotation stage and is therefore not needed further.

25

Figure 3 shows one possible embodiment of the data rotator 100.

The received data signal is input in a rectangular co-ordinate form with the X co-ordinate, X_n , being input at 3a and the Y co-ordinate, Y_n , being input at 3b.

30

The data rotator comprises two adders, 10 and 11, which are controlled by way of the adder control signal 13, two shift registers, 18 and 19, which are controlled by way of the shift control signal 30, two multiplexers, 22 and 23, which are controlled by way of the multiplex control signal 29, and another two multiplexers, 26 and 27, which are controlled by way of the load control signal 28. The control signals 13, 28, 29, 30 and 31 are supplied by the

control section 12 as shown in Figure 5. Additionally there are two registers, 6 and 7, which are used to store the current X and Y co-ordinate values of the data signal. The adder control signal, 13, is fed via an inverter, 15, before being input to adder 10. This has the effect that the adder 10 and the adder 5 11 are generally performing the opposite function - i.e. if the adder 10 is adding, the adder 11 is subtracting, and vice versa.

Depending on the value of the load control signal 28, the multiplexer 26 is used to either load a new X co-ordinate into the register 6, or to load the 10 output of the adder 10 into the register 6. The multiplexer 27 performs the same operation for the Y co-ordinate and causes either a new Y co-ordinate or the output of the adder 11 to be loaded into the register 7, depending on the value of the load control signal 28.

15 Similarly, the multiplexer 22, under control of the multiplexer control signal 29, allows either a zero or the contents of the register 6 to be fed into the adder 10. The multiplexer 23, under control of the multiplexer control signal 29, allows either a zero or the contents of the register 7 to be fed into the adder 11.

20 The shift registers 18 and 19 shift their respective data to perform a division by 1, 2, 4, 8 etc. according to the value of the shift control signal 30.

25 The pass control signal 31 is input to adders 8, 9, 10 and 11 and allows the adders to perform a pass-through function (i.e. it causes the adders to pass through the data and not to perform any addition or subtraction). This is used in the event that the Y co-ordinate reaches zero quickly, the 'rotation' process can continue for a given number of cycles without affecting the data before the rotation process is deemed complete. This has the desirable effect of 30 keeping the number of cycles required to obtain a result substantially constant.

The operation of the data vector rotator is controlled by the control section 104, which is described in more detail later.

At the end of the rotation operation, after the required number of iterations 5 has been performed, both the X and Y co-ordinates are transferred to the scalar divider section 103.

Figure 4 is a diagram showing a detailed view of the scalar divider according to the present invention. The X co-ordinate of the corrected reference signal, 10 X_d , is input to a divider register 39, under control of a load signal 41. The X and Y co-ordinates of the corrected data signal, X_n and Y_n , are input to a register 34 and a register 36 respectively, again under control of the load signal 41. The scalar divider 103 further comprises two adders, 37 and 38, two inverters, 42 and 43, and a further two registers, 33 and 35. The adders 15 37 and 38 are controlled by control signals 45 and 44 respectively which are responsible for changing the function of the adders from addition to subtraction according to the values of the control signals.

The operation of the scalar divider is controlled by the control section 104, 20 and at the end of the operation, the X and Y co-ordinates of the fully corrected data signal, in complex form as $X_q + jY_q = \frac{X_n + jY_n}{X_d + jY_d}$, are output at 48 and 49 respectively.

Figure 5 shows the inputs and outputs of the control section 104. A start 25 signal 1 indicates when new reference and data signals are available and this is used as the trigger to start the correction process.

The correction process is performed in accordance with the procedures described by the flow diagrams shown in Figure 6a and 6b. Figure 6a 30 describes the first cycle of the operation, which causes a 90-degree rotation of the vectors. Figure 6b describes the operation of subsequent cycles which

results in further rotations of the vectors, either until the Y co-ordinate is equal to zero, or until a fixed number of cycles, or iterations, have been performed. The control section 104 generates control signals as appropriate, during the course of processing, to control the actions of the reference signal rotator 5 100, the data signal rotator 101 and the scalar divider 103.

Once the rotation stage is complete, the phase corrected data vector is scalar divided by the phase corrected reference vector resulting in the data vector being corrected for both phase and amplitude.

10

A worked example of the rotation stage is shown below in Table 1.

Step	Reference X	Reference Y	Data X	Data Y	Comments
Input	5	10	7	-4	input values
1	10	-5	-4	-7	$X := Y; Y := -X$
2	13	5	3	-11	$X := X-Y; Y := Y+X$
3	16	-1	-2	-12	$X := X+Y/2; Y := Y-X/2$
4	16	3	1	-12	$X := X-Y/4; Y := Y+X/4$
5	16	1	0	-12	$X := X+Y/8; Y := Y-X/8$
6	16	0	-1	-12	$X := X+Y/16; Y := Y-X/16$
7	16	0	-1	-12	Process halted, as $Y = 0$
8	16	0	-1	-12	Process halted, as $Y = 0$
9	16	0	-1	-12	Process halted, as $Y = 0$

Table 1

15 The X and Y co-ordinates of the data vector are then available for further processing as required.

Figure 7 shows an example (not to scale) of a rotation of a reference vector according to the method described above. It can be seen that each rotation is

progressively diminishing in size and also causes an increase in the length of the reference vector. Although Figure 7 shows that with each rotation, the Y co-ordinate of the reference vector changes sign; this may not always be the case depending on the initial value.

5

It will be appreciated by anyone skilled in the art that the present invention is not limited, however, just to the method as describe above. In an alternative embodiment the process can be implemented entirely in software, through use of an appropriately programmed microprocessor or other computing means. In a yet another embodiment, the two rotators (i.e. the reference vector rotator and the data vector rotator) can be replaced by a single rotator which is used first to rotate the reference vector and then used to rotate the data vector by the same amount. This would have the effect of further reducing the amount of hardware or software to implement the present invention.

15 It will also be appreciated that references to vector division could also encompass complex division techniques.

Claims:

1. A method of recovering the amplitude and phase of an input data signal including at least one data vector and a reference vector, so as to reduce the effect of distortion on the input data signal, the method comprising the following steps:
 - 5 rotating the reference vector;
 - rotating the data vector by reference to the rotation of the reference vector; and
 - 10 dividing the rotated data vector by the rotated reference vector; thereby recovering the phase and amplitude of the input data signal.
2. A method according to claim 1, wherein the step of rotating the vectors comprises rotating by a plurality of sub-steps of progressively diminishing size.
 - 15
3. A method as claimed in claim 1 or 2, further comprising representing the vectors digitally and in the form of a pair of co-ordinate values.
 - 20
4. A method as claimed in claim 3, wherein a first step in the rotation of each vector comprises combining the co-ordinate values by a process of addition to rotate the vector through an angle of predetermined magnitude.
 - 25
5. A method as claimed in claim 4, wherein subsequent steps in the rotation of each vector comprise combining the co-ordinate values by a process of addition and multiplication to rotate the vectors through progressively smaller angles.
 - 30
6. A method as claimed in any one of claims 2 to 5 further comprising stopping the rotation sub-steps if the reference vector is rotated to a predetermined angle.

7. Apparatus for recovering the amplitude and phase of an input data signal including at least one data vector and a reference vector comprising:

5 a rotator for rotating the reference vector and for rotating the data vector with reference to the reference vector; and
a divider for dividing the two vectors; thereby recovering the phase and amplitude of the input data signal.

10 8. Apparatus as claimed in claim 7, wherein the rotator comprises one or more mathematical operators.

15 9. Apparatus as claimed in claim 7 or 8, wherein means are provided to detect whether the reference vector has been rotated to a predetermined angle.

10. Apparatus as claimed in claim 7, 8 or 9, including a controller to control the sequence of steps performed by the rotator and the divider.

20 11. Apparatus as claimed in claim 7, 8, 9 or 10 adapted to rotate and divide two vectors represented digitally in the form of a pair of co-ordinate values.

25 12. Apparatus as claimed in claim 11 wherein a digital shift register is provided to selectively halve the value of one of the vector co-ordinates.

13. Apparatus as claimed in any one of claims 7 to 12, wherein the divider is a scalar divider.

30 14. Apparatus as claimed in any one of claims 7 to 13, further comprising a plurality of rotators, one for each vector.

15. A method of transmitting a data signal including at least one data vector and a reference vector, which data signal is adapted to be recovered by the method of any of claim 1-6.

5

16. Apparatus for transmitting a data signal including at least one data vector and a reference vector, which apparatus is adapted such that the data signal can be recovered by the apparatus of any of claim 7-14.

Fig.1.

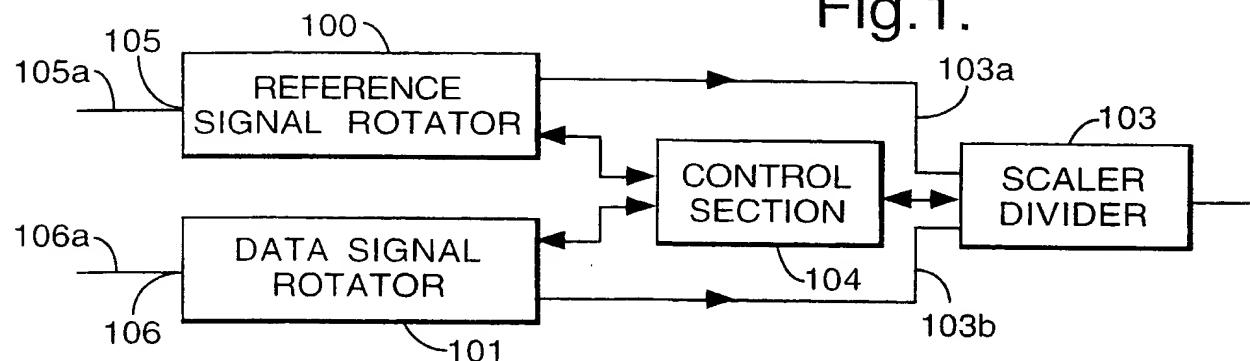


Fig.2.

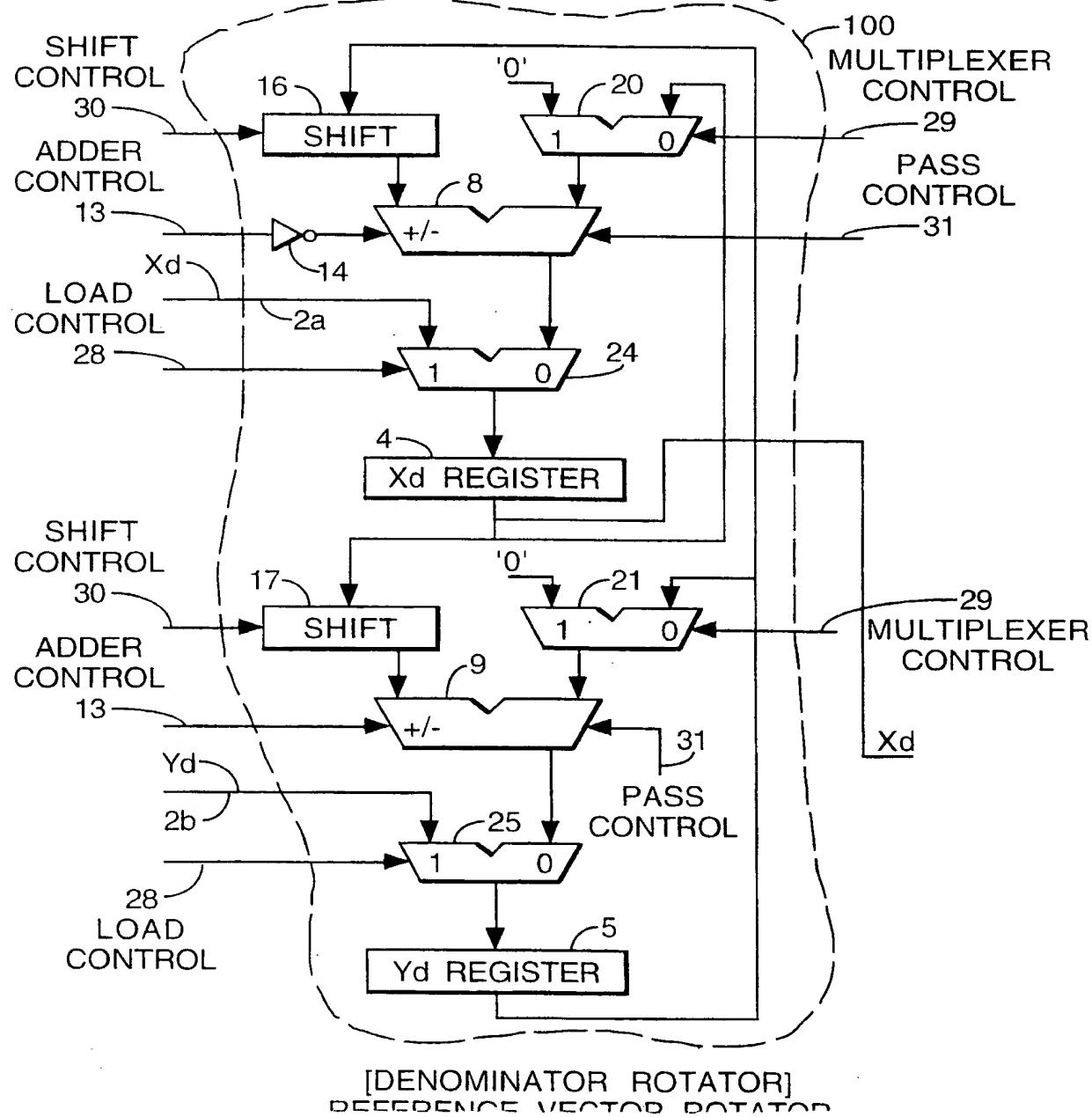


Fig.3.

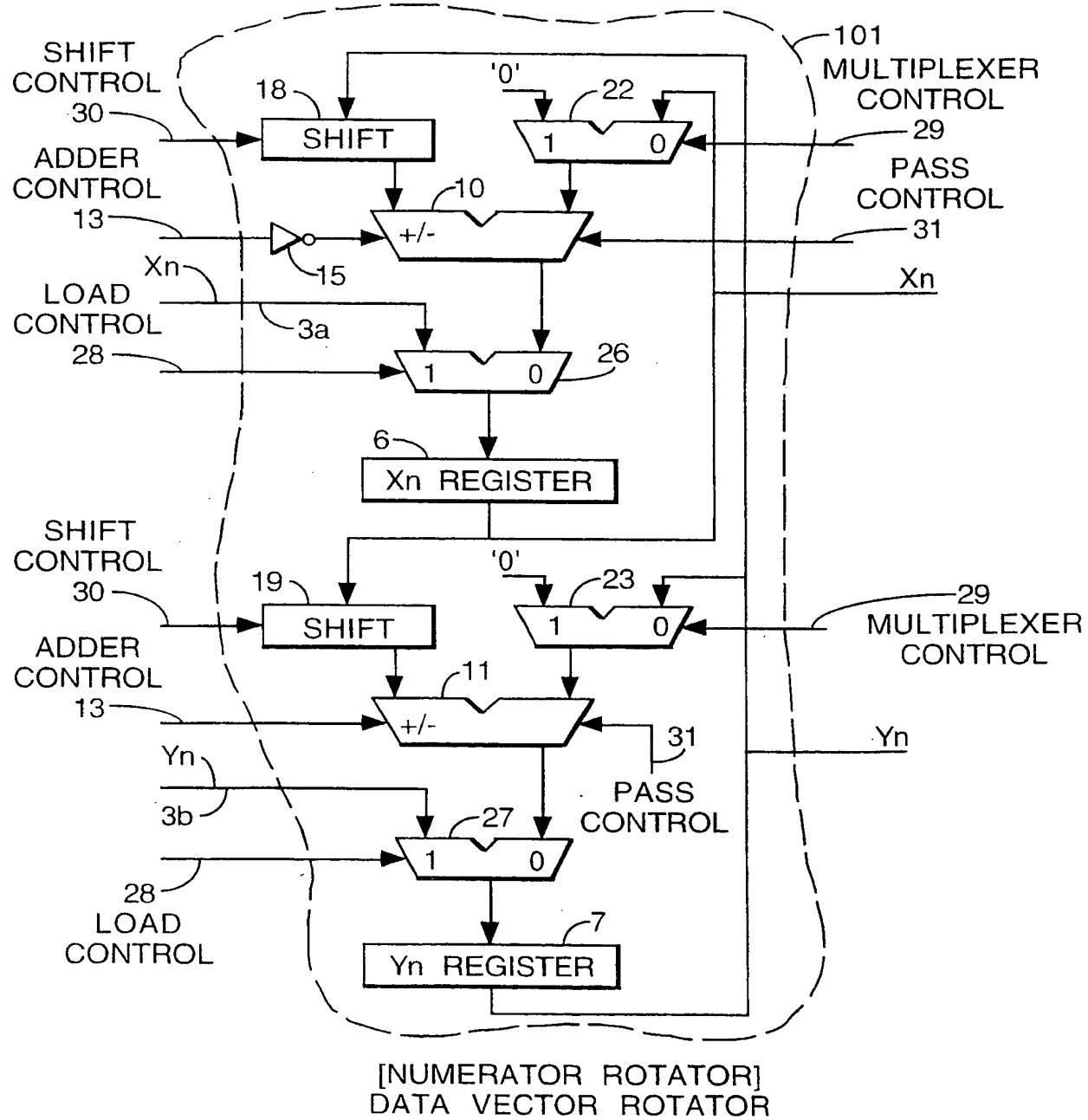


Fig.4.

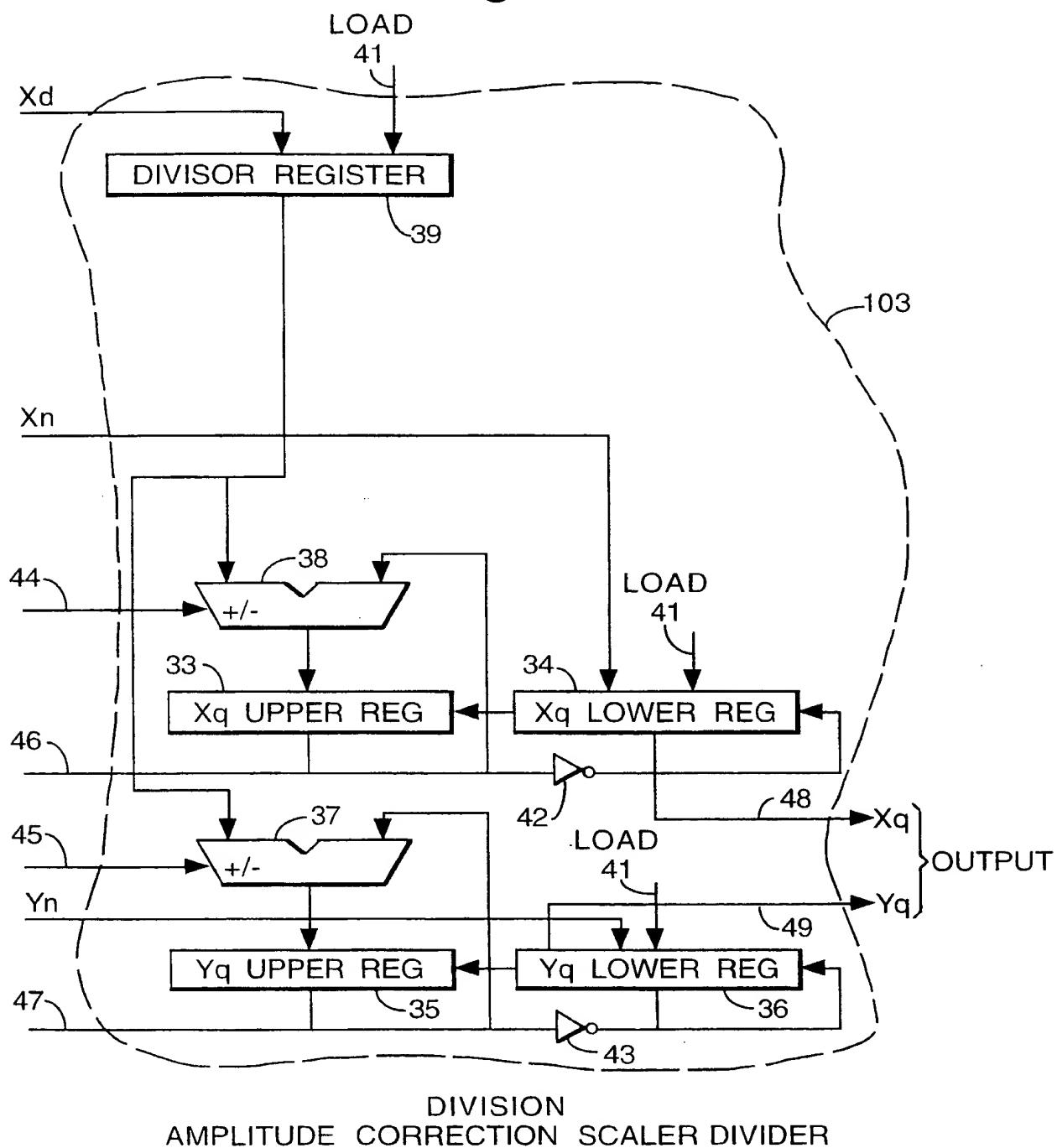


Fig.5.

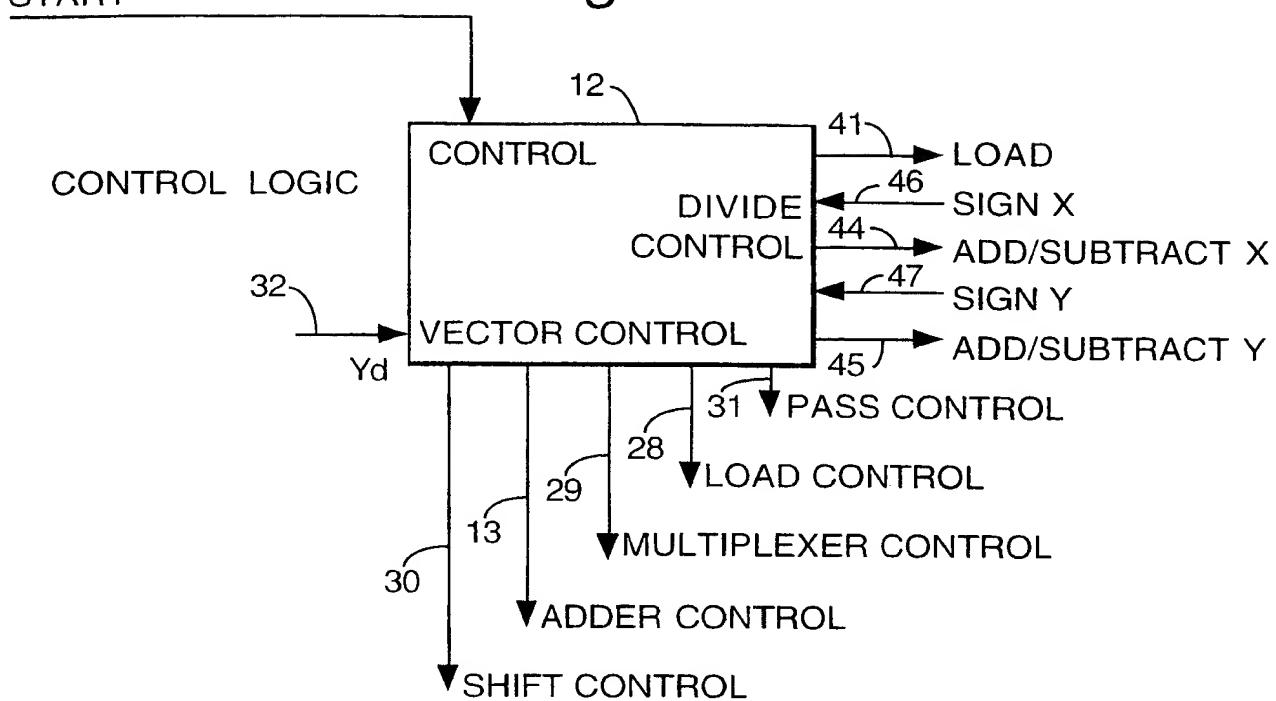


Fig.6a.

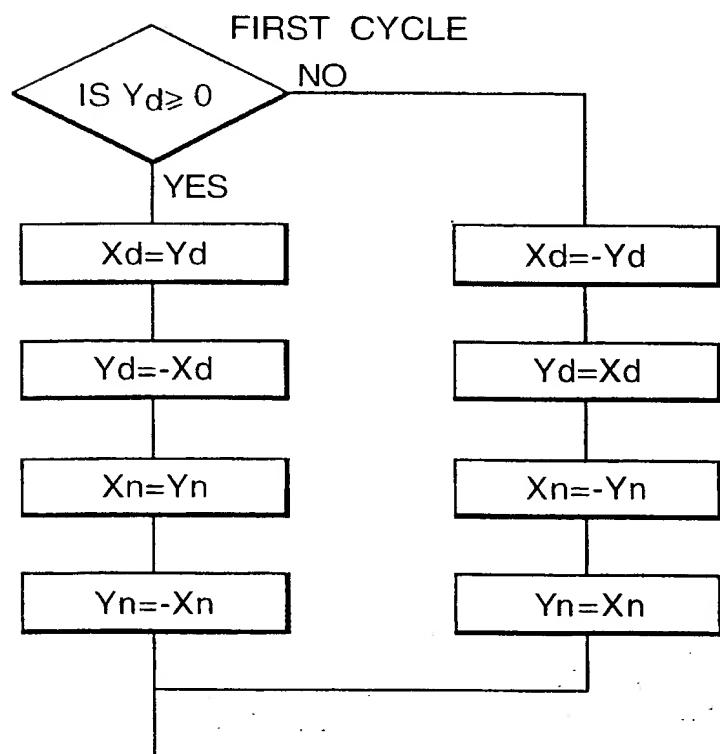


Fig.6b.

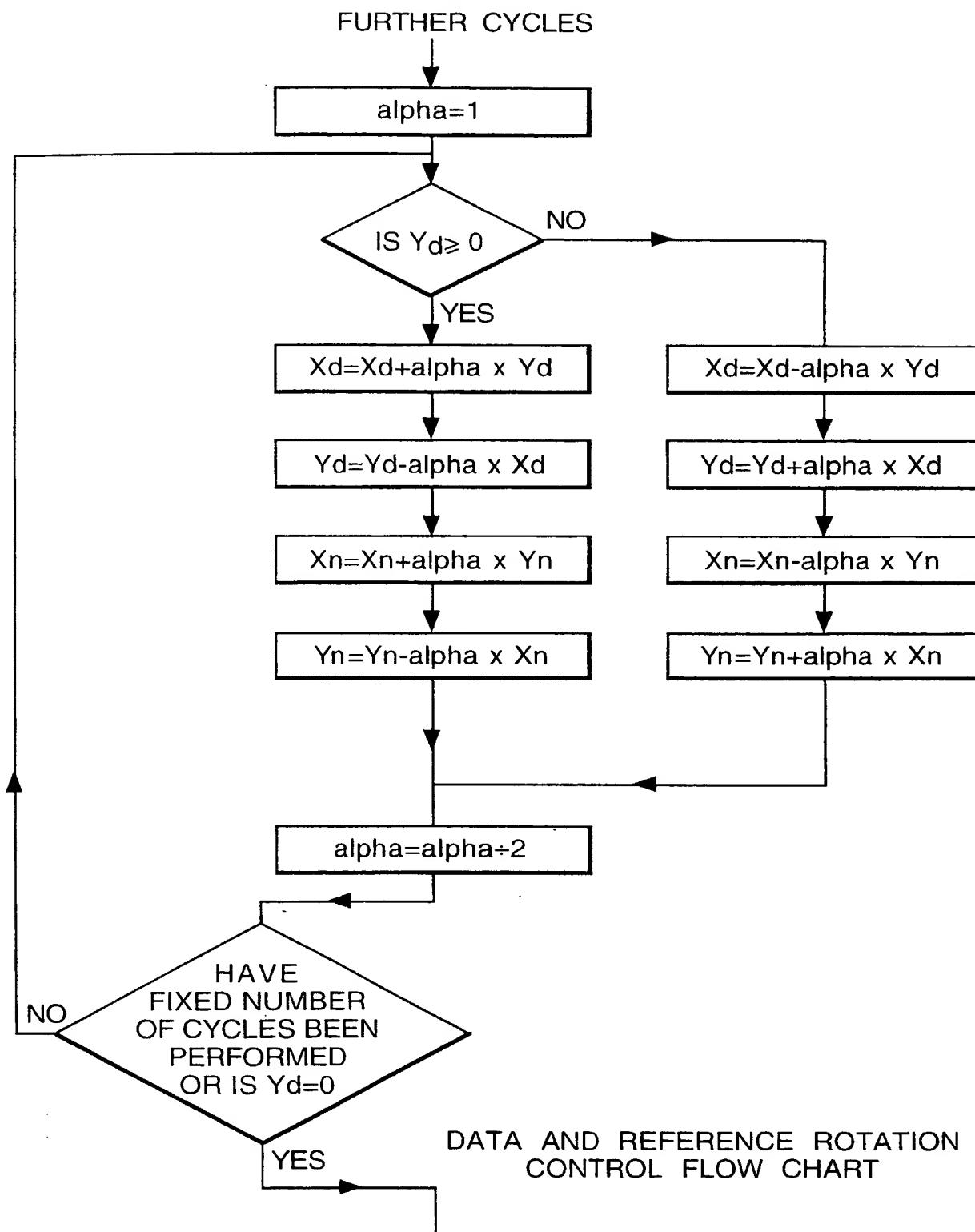
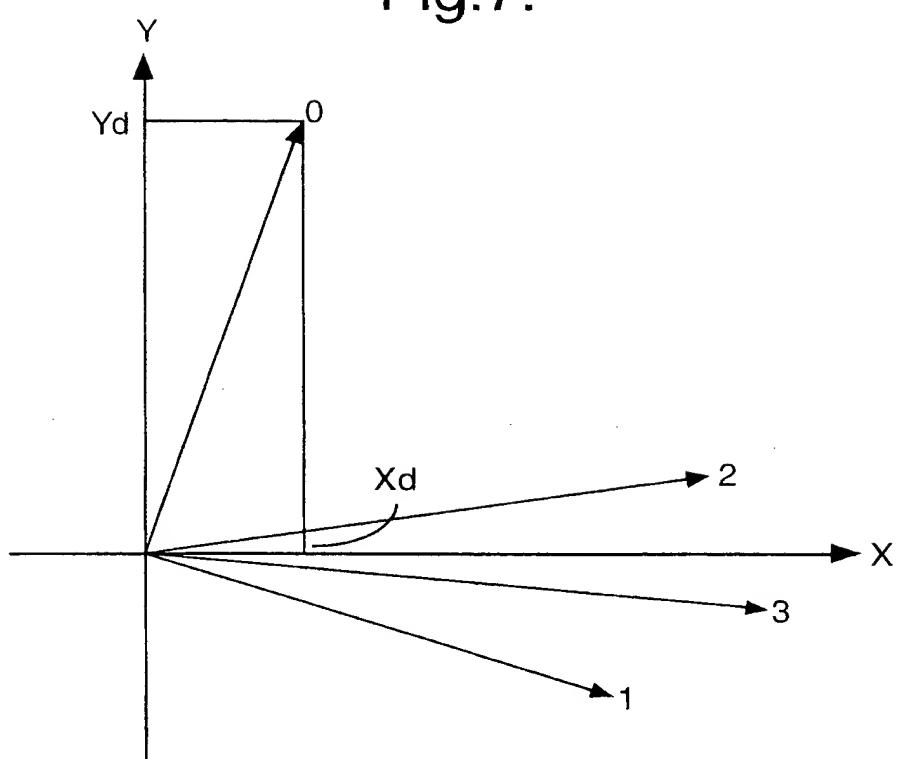


Fig.7.



INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 98/00323

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 H04L27/26 H04L27/233 H04L27/38

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A		1,3,7,8, 15,16
A		1,3,7,8, 15,16

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Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
 NL 2280 HV Rijswijk
 Tel. (+31-70) 340-2040, Tx. 31 651 epo nl
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Authorized officer

Scriven, P

INTERNATIONAL SEARCH REPORT

Internat'l Application No

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